Petition Copy of #8

MYERS DAWES & ANDRAS LLP

PATENTS, TRADEMARKS AND COPYRIGHTS

FACSIMILE TRANSMITTAL SHEET

TO:	FROM:
Examiner D. Graybill	**Joseph Andras**
COMPANY:	DATE: **March 22, 2002**
FAX NUMBER: **703-308-7724**	TOTAL NO. OF PAGES INCLUDING COVER: **31**
PHONE NUMBER:	SENDER'S REFERENCE NUMBER: **IRV1.PAU.30**
RE: **Appl. No. 09/190,378**	YOUR REFERENCE NUMBER: **Group Art Unit: 2814**

Copy of petition to withdraw Abandonment 1/10/02

☐ URGENT ☐ FOR REVIEW ☐ PLEASE COMMENT ☐ PLEASE REPLY ☐ PLEASE RECYCLE

NOTES/COMMENTS:

FAX COPY RECEIVED
MAR 2 2 2002
TECHNOLOGY CENTER 2800

ATTENTION: Examiner D. Graybill

Re: Application of: Douglas M. Albert, Volkan H. Ozguz
Serial No.: 09/190,378
Filed: November 10, 1998
For: **METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME**

Attached are the Request for Withdrawal of Notice of Abandonment and related documents forwarded to the Patent Office on December 14, 2001 and processed on January 10, 2002 by the Patent Office as date stamped on the return postcard, copy attached.

Thank you for your help,

I hereby certify that this correspondence for patent application no. 09/190,378 is being facsimile transmitted to the Patent and Trademark Office fax number (703) 308-7724 on

March 22, 2002

By Angela Williams

Signature

March 22, 2002

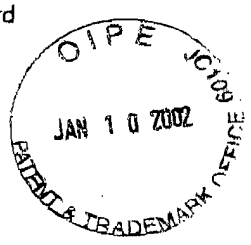
19900 MACARTHUR BOULEVARD, SUITE 1150, IRVINE, CA 92612
PHONE: (949) 223-9600 FAX: (949) 223-9610
WWW.MDALAW.COM

The official stamp of the PTO hereon acknowledges receipt of:

Date: December 14, 2001
Serial No.: 09/190,378
Filed: November 10, 1998
Client: IRVINE SENSORS CORP.
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME
Atty. Dkt. No.: IRV1.PAU.30

Enclosed:

1. Request for Withdrawal of Notice of Abandonment Or, in the Alternative, Petition to Revive (2 pages)
2. Declaration of Joseph C. Andras (2 pages) + attachment
3. Return Postcard



Docket No. IRV1.PAU.30 **Patent Application**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Douglas M. Albert, Volkan H. Ozguz	Examiner: David E. Graybill
Serial No.: 09/190,378	Group Art Unit: 2814
Filed: November 10, 1998	
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine, California December 14, 2001

REQUEST FOR WITHDRAWAL OF NOTICE OF ABANDONMENT OR, IN THE ALTERNATIVE, PETITION TO REVIVE

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Applicant recently received the attached Notice of Abandonment and respectfully submits the herein Request For Withdrawal Of Notice Of Abandonment Or, In The Alternative, Petition To Revive.

As set forth in more detail in the attached Declaration of Joseph C. Andras, the case should not have gone abandoned as the Applicant filed a timely Response on October 22, 2001. It appears that the Patent Office simply did not receive such response (presumably in light of the mail-related issues of late).

Applicants respectfully request that the abandonment be withdrawn.

If necessary, however, Applicants request that this paper be treated as a Petition to Revive on the basis that the application was unavoidably abandoned as provided for by Subsection (a) of Rule 137. In that event, please charge any related fees, including the petition fee required by 37 CFR § 1.17(l), and refund any overpayment to our deposit account no. 01-1960.

Thank you for your consideration.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on December 14, 2001

Angela Williams

Signature
December 14, 2001

Respectfully submitted,

Joseph C. Andras
Registration No. 33,469
Myers Dawes & Andras LLP
19900 MacArthur Blvd, Suite 1150
Irvine, CA 92612

Docket No. IRV1.PAU.30 **Patent Application**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Douglas M. Albert, Volkan H. Ozguz	Examiner: David E. Graybill
Serial No.: 09/190,378	Group Art Unit: 2814
Filed: November 10, 1998	
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine, California December 13, 2001

DECLARATION OF JOSEPH C. ANDRAS

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I, Joseph C. Andras, hereby declare as follows:

1. I am an attorney admitted to practice law in the State of California and the attorney of record in U.S. Patent Application No. 09/190,378 entitled "Method For Thinning Semiconductor Wafers With Circuits And Wafers Made By The Same."

2. Attached hereto under Tab "A" is a copy of the Notice of Abandonment that we just received.

3. Attached hereto under Tab "B" is a true and correct copy of the papers that we filed on October 22, 2001, in response to the Office Action of April 20, 2001, including: (1) a response entitled AMENDMENT "A"; (2) Declaration of Douglas M. Albert; (3) Declaration of Inventor Volkan H. Ozguz; (4) a Request for Three-Month

Extension of Time; (5) a check to cover the extension fee in the amount of $460.00; and (6) a postcard listing all the foregoing items.

4. In view of the fact that we timely filed the attached Response, it is respectfully submitted that the abandonment was issued in error or that the application has been unavoidably abandoned. We respectfully request, therefore, that the Office withdraw the abandonment or revive the application.

I declare under penalty of perjury that the foregoing is true and correct.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on December 14 2001
Angela Williams

Signature
December 14 2001

Respectfully submitted,

Joseph C. Andras
Registration No. 33,469
Myers Dawes & Andras LLP
19900 MacArthur Blvd, Suite 1150
Irvine, CA 92612

B

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/190,378	11/10/1998	DOUGLAS M. ALBERT	IRV1.PAU.30	6576

7590 11/26/2001

JOSEPH C ANDRAS
650 TOWN CENTER DRIVE
SUITE 650
COSTA MESA, CA 92626

EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/26/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

TAB 'A'

BN

Notice of Abandonment	Application No. 09/190,378	Applicant(s) ALBERT, DOUGLAS M.	
	Examiner David E Graybill	Art Unit 2814	

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address–

This application is abandoned in view of:

1. ☒ Applicant's failure to timely file a proper reply to the Office letter mailed on *20 April 2001*.
   (a) ☐ A reply was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply (including a total extension of time of _____ month(s)) which expired on _____.
   (b) ☐ A proposed reply was received on _____, but it does not constitute a proper reply under 37 CRF 1.113 (a) to the final rejection.
   (A proper reply under 37 CRF 1.113 to a final rejection consists only of: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114).
   (c) ☒ No reply has been received.

2. ☐ Applicant's failure to timely pay the required issue fee and publication fee, if applicable, within the statutory period of three months from the mailing date of the Notice of Allowance (PTOL-85).
   (a) ☐ The issue fee and publication fee, if applicable, was received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the statutory period for payment of the issue fee (and publication fee) set in the Notice of Allowance.
   (b) ☐ The submitted fee of $_____ is insufficient. A balance of $_____ is due.
   The issue fee required by 37 CFR 1.18 is $_____. The publication fee, if required by 37 CFR 1.18(d), is $_____.
   (c) ☐ The issue fee and publication fee, if applicable, has not been received.

3. ☐ Applicant's failure to timely file new formal drawings as required by, and within the three-month period set in, the Notice of Allowability (PTO-37).
   (a) ☐ Proposed new formal drawings were received on _____ (with a Certificate of Mailing or Transmission dated _____), which is after the expiration of the period for reply.
   (b) ☐ The proposed new formal drawings filed on _____ are not acceptable and the period for reply has expired.
   (c) ☐ No proposed new formal drawings have been received.

4. ☐ The letter of express abandonment which is signed by the attorney or agent of record, the assignee of the entire interest, or all of the applicants.

5. ☐ The letter of express abandonment which is signed by an attorney or agent (acting in a representative capacity under 37 CFR 1.34(a)) upon the filing of a continuing application.

6. ☐ The decision by the Board of Patent Appeals and Interference rendered on _____ and because the period for seeking court review of the decision has expired and there are no allowed claims.

7. ☐ The reason(s) below:

David E Graybill
Primary Examiner
Art Unit 2814

The official stamp of the PTO hereon acknowledges receipt of:

Date: October 22, 2001
Serial No.: 09/190,378
Client: IRVINE SENSORS
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME
Atty. Dkt. No.: IRV1.PAU.30

Enclosed:

1. Amendment "A" (12 pages)
2. Declaration of Douglas M. Albert (6 pages)
3. Declaration of Inventor Volkan H. Ozguz (2 pages)
4. Request for Three-Month Extension of Time (1 page + duplicate)
5. Check No. 4401 in the amount of $460.00
6. Return Postcard

TAB 'B'

Docket No. IRV1.PAU.30 **Patent Application**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Douglas M. Albert Volkan H. Ozguz Serial No.: 09/190,378 Filed: November 10, 1998 For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Examiner: D. Graybill Group Art Unit: 3722 Irvine, California October 22, 2001

AMENDMENT "A"

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Please enter the following amendment in response to the Office Action dated April 20, 2001.

In the Claims

Please cancel Claims 25-27 directed to a non-elected product without prejudice. Applicants may elect to prosecute such claims in a divisional application.

The claims that are amended as shown in the attached Appendix appear in clean form as follows:

1. (Twice Amended) A method for manufacturing a plurality of dies containing thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

defining a plurality of grooves into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer;

mounting said wafer to a flat rigid substrate to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate;

mechanically removing a predetermined portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining mounted to said substrate; and

releasing said plurality of dies from said substrate.

2. (Amended) The method of claim 1 further comprising disposing a planarizing layer of material on said front surface of said wafer into which said plurality of grooves have been defined prior to mounting said front surface of said wafer to said flat substrate.

3. (Amended) The method of claim 1 further comprising disposing a layer of material on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

10. (Amended) The method of claim 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of an adhesive.

13. (Amended) The method of claim 1 further comprising mounting a die from said plurality of dies onto a flexible film.

15. (Amended) The method of claim 13 where mounting said die on said flexible film further comprises electrically coupling an integrated circuit in said die to metalizations provided on said film.

18. (Amended) The method of claim 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using an adhesive material disposed between said front surface and said flat substrate

19. (Amended) The method of claim 18 further comprising pressing said wafer and substrate together with said adhesive material therebetween and curing said adhesive material while maintaining said pressure between said wafer and substrate.

23. (Amended) The method of claim 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said plurality of dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

24. (Amended) The method of claim 1 further comprising stacking a plurality of dies manufactured by said method, and electrically interconnecting said plurality of dies.

REMARKS

This amendment is responsive to the Office Action dated April 20, 2001. Attached hereto, therefore, are a request for a three-month extension of time and the appropriate fee.

Claims 1-24 and 28-32 are now pending. The Office Action rejects certain claims under 35 U.S.C. 112, second paragraph, rejects Claims 1, 2, 7-9, 13, 20, 21 and 23 under 35 U.S.C. 102(e)[1] as anticipated by U.S. Patent No. 6,083,811 to Riding, and rejects various other claim groups under 35 U.S.C. 103(a) as obvious over Riding in combination with one or more additional references.

Section 112 Rejections

Applicants have carefully amended certain ones of the claims to address each of the Examiner's Section 112 concerns:

Applicants have amended the preamble of Claim 1 to recite "a plurality of dies" to provide antecedent support for the reference to "said" plurality of dies at line 7 of amended claim 1.

[1] The Office Action indicates that the rejections is based on 35 USC 102(b), but during a telephone conference with Applicants' attorney, the Examiner kindly confirmed that the applicable section is 102(e), not 102(b).

Applicants have amended Claims 13, 23 and 24 to provide literal antecent basis for "said dies". In particular, Claim 13 now introduces "a die" that is "from said plurality of dies" and Claims 23 and 24 reference "said plurality of dies".

Applicants have resolved the antecedent problem with the reference to "said die" in Claims 14-16 by amending parent Claim 13 to introduce "a die" as noted above.

Applicants have resolved the antecedent problem with "said integrated circuit" in Claim 15 by amending the claim to recite "an integrated circuit".

Applicants have resolved the antecedent problem with Claim 16 by amending Claim 15 as just noted.

Applicants have resolved the antecedent problem with Claim 16's use of the phrase "a plurality of separated dies prepared by said method" to read "a plurality of dies manufactured by said method".

Finally, with regard to the use of the terms "low" in Claims 2, 3, 10, 18 and 19, Applicants have simply deleted those limitations from the claims. Claim 2, for example, now recites "a planarizing layer of material" rather than "a planarizing layer of *low stress* material".

The Examiner is invited to telephone the undersigned attorney if any further Section 112 concerns become apparent.

Rejections Based on Riding

As noted in the introductory portion of these remarks, all of the Office Action's rejections rely upon Riding as prior art. The Riding reference corresponds to U.S. Patent No. 6,083,811. It issued on July 4, 2000, long after the November 11, 1997 filing date of the provisional patent application no. 60/065,088 to which Applicants' claim benefit. Accordingly, the Riding patent is available as a prior art reference under 35 U.S.C. 102(e) based on its filing date. The "effective date" of the Riding patent, in other words, is February 7, 1996.

In accordance with the applicable statutes and rules therefore, Applicants have elected to swear behind Riding by submitting declarations that provide substantial evidence that their herein claimed invention was invented prior to the effective date of the Riding patent. That reference no longer being applicable as a prior art reference, it appears that the present case is substantively in condition for allowance.

Conclusion

It now appearing that this case is fully in condition for allowance, Applicants earnestly solicit a notice to that effect. Applicants invite the Examiner to call the undersigned attorney if it appears that a phone conference would further this case in any way.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on
October 22, 2001
Angela Williams

A. Williams
Signature
October 22, 2001

Respectfully submitted,

Joseph C. Andras
Registration No. 33,469
Myers, Dawes & Andras LLP
19900 MacArthur Blvd, Suite 1150
Irvine, CA 92612

Appendix of Amended Claims With Amendments Shown

1. (Twice Amended) A method for manufacturing a plurality of **dies containing** thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:

defining a plurality of grooves into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said surface at a predetermined distance less than said thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer;

mounting said wafer to a flat rigid substrate to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate;

mechanically removing a predetermined portion of said backside of said wafer until said thickness of said wafer is reduced to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining mounted to said substrate; and

releasing said plurality of dies from said substrate.

2. (Amended) The method of claim 1 further comprising disposing a planarizing layer of ~~low stress~~ material on said front surface of said wafer into which said plurality of grooves have been defined prior to mounting said front surface of said wafer to said flat substrate.

3. (Amended) The method of claim 1 further comprising disposing a layer of ~~low stress~~ material on said front surface of said wafer before defining said plurality of grooves into said front surface of said wafer.

10. (Amended) The method of claim 1 wherein mounting said wafer to said flat substrate comprises affixing said wafer by means of ~~a low viscosity low stress~~ an adhesive.

13. (Amended) The method of claim 1 further comprising mounting a die from said plurality of dies onto a flexible film.

15. (Amended) The method of claim 13 where mounting said die on said flexible film further comprises electrically coupling ~~said~~ an integrated circuit in said die to metalizations provided on said film.

18. (Amended) The method of claim 17 wherein affixing said front surface to said flat substrate comprises affixing said front surface using ~~low viscosity, low stress materials~~ an adhesive material disposed between said front surface and said flat substrate.

19. (Amended) The method of claim 18 further comprising pressing said wafer and substrate together with said ~~low viscosity and low stress~~ **adhesive** material therebetween and curing said **adhesive** material while maintaining said pressure between said wafer and substrate.

23. (Amended) The method of claim 1 where defining said plurality of grooves in said front surface of said wafer comprises defining linear grooves into said front surface of said wafer in an intersecting grid pattern to define each of said **plurality of** dies, thereby isolating each die by a surrounding moat of stress relieving grooves.

24. (Amended) The method of claim 1 further comprising stacking a plurality of ~~separated~~ dies ~~prepared~~ **manufactured** by said method, and electrically interconnecting said **plurality of** dies.

~~25. (Cancel) An assembly used for manufacturing a plurality of thinned integrated circuits from a semiconductor wafer having a thickness, a front surface and a backside surface, comprising:~~

~~a plurality of grooves defined into said front surface of said semiconductor wafer to define said plurality of dies, said grooves penetrating into said front surface a predetermined distance which is less than said~~

~~thickness of said semiconductor wafer so that said plurality of dies remain integral with said wafer; and~~

~~a flat rigid substrate mounted to said wafer to support said wafer, said wafer being mounted to said substrate with said front surface turned toward said substrate and to expose said backside of said wafer for partial mechanical removal of said backside by an amount sufficient to expose said plurality of grooves to said backside in preparation to separating said plurality of said dies, said dies remaining of mounted to said substrate.~~

~~26. (Cancel) The assembly of claim 25 further comprising a low viscosity, low stress layer disposed between said front surface of said wafer and said substrate to affix said front surface of said wafer to said substrate.~~

~~27. (Cancel) The assembly of claim 25 wherein said low viscosity, low stress layer includes a polyimide layer disposed on said front surface.~~

Docket No. IRV1.PAU.30 **Patent Application**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :	Examiner: D. Graybill
Douglas M. Albert et al.	Group Art Unit: 3722
Serial No.: 09/190,378	
Filed: November 10, 1998	
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine, California
	October 22, 2001

DECLARATION OF DOUGLAS M. ALBERT
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

I, Douglas M. Albert, hereby declare as follows:

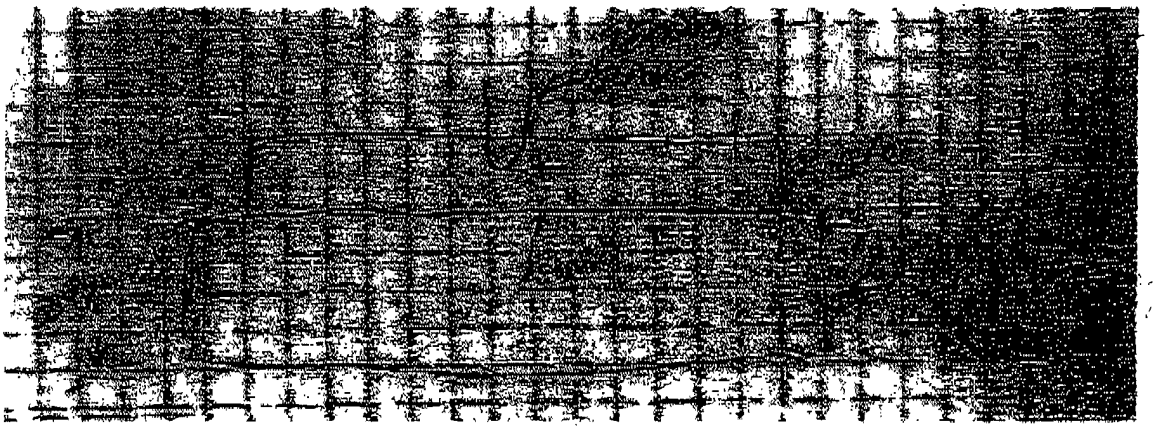
1. I am a co-inventor of the invention disclosed and claimed in patent application no. 09/190,378. I am making this declaration to establish facts showing that the invention claimed in this application was reduced to practice before February 7, 1996, which I am informed is the filing date of the application that issued to Alan J. Riding et al. as U.S. Patent No. 6,083,811 ('811 Patent). I will hereinafter refer to February 7, 1996 as the "Effective Date" of the '811 Patent.

2. I am employed by the assignee, Irvine Sensors Corporation ("ISC"). I work at ISC's Costa Mesa facility in the State of California. I have been employed continuously by ISC at all times relevant hereto

3. I have read Claims 1-32 that are pending in this application and have a technical understanding of how such claims apply to the disclosure of this application. As shown by the exhibits that I have attached hereto, Mr. Ozguz and I developed the method for thinning semiconductor wafers that is described and claimed in our patent application before the Effective Date of the '811 Patent.

4. Attached hereto as Exhibit A, for example, is a page from my inventor's notebook entitled "Grinding with Diced Wafers", dated "7/27/95", which describes and illustrates the claimed invention as follows:

> Theory – Dice wafers partially through leaving 10 mil of [silicon] between bottom of cut and bottom of wafer. After dicing, mount wafer to substrate and grind past depth of dicing cut, therefore leaving chips mounted to substrate as opposed to a wafer.



5. At the bottom of Exhibit A are detailed observations regarding three actual "results", i.e. evidence of an actual reduction to practice of our claimed invention at least as of July 27, 1995, prior to the Effective Date of the '811 Patent.

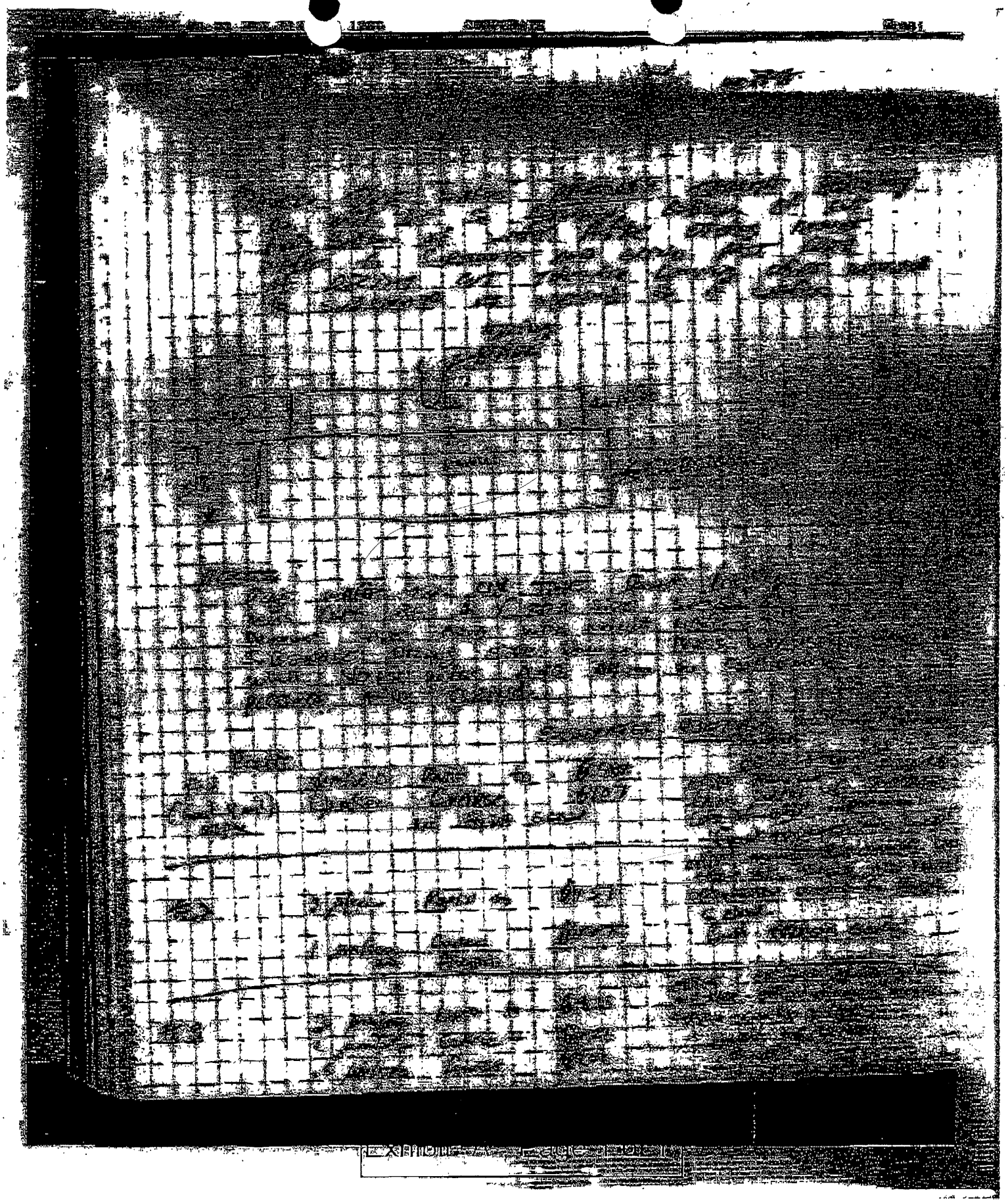
6. Also attached hereto as Exhibit B is a written "Status Report" that I prepared on or about "8-1-95". The memo further corroborates our having successfully back-ground partially diced wafers, in the manner claimed in our patent application, prior to the Effective Date of the '811 Patent.

7. This declaration factually establishes that the claimed invention was reduced to practice in the United States prior to the Effective Date of the '811 Patent.

8. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

10/19/2001
Date

Douglas M. Albert



HDIOI STATUS REPORT

PRIME SENSORS CORP.

Subject: Present Wafer Thinning Experiment Status
To: Angel Pepe, Dave Ludwig
From: Doug Albert
Date: 8-1-95
CC: E.G., Y.R.

Conclusion:

Based on my experiments up to this point it appears clear to me that in order to ultimately thin wafers to 10 µm a wafer backing medium will be necessary. The challenge I was handed was to see how thin a 3" wafer could be mechanically be ground. Considering there really was no spec. established for mechanical grinding, my goal was to go as thin as possible. The initial thoughts of mounting and grinding wafers on UV tape and processing them on the tape now look dismal. The thinnest wafer that was ground with NO breakage was 4 mils and even that is NOT repeatable. Also, demounting the UV tape from a wafer that is very thin proved very difficult and seems to me a high risk approach.

A second approach was to mount a wafer to a substrate with some sort of adhesive then thin and process the wafer on the substrate. Presently this method is working fairly well. I have been thinning 4" wafers submounted to Macor substrates using a variety of adhesives. I have successfully thinned and demounted 2 mil wafers and ground 1 wafer to 20 µm (not demounted). The process does appear to be pretty repeatable. By far the most touchy area is demounting and propagation of cracking from wafer edge. Note: The program calls for thinning 3" wafers for which the substrates are on order. Until proper substrates are received and tried nothing is for sure.

To go one step further, in order to eliminate crack propagation across a wafer and isolate chips within a substrate a chip isolation process was born. By dicing partially through a wafer, mounting the diced surface down toward the substrate and grinding down past the diced grooves, chips were created hence eliminating crack propagation. This also creates chips alleviating the need to create chips using a lithographic process using plasma etching. I am still working some small movement problems with this process. I am also still establishing my thinning limits with this process as well.

All in all things look positive. I am continuing with experiments and will have a more in depth report upon completion of the experiments. I presently do not see any major roadblocks. I am confident that the present problems can be solved.

Diced Submount Thinning

The next step was to see if we could eliminate the need to dice streets after the thinning in order to create chips. By performing the chip isolation early in the process we now will only lose a chip in the event of a crack or breakage. The way this was performed was to dice partially into a wafer mount the diced side down and backgrind the wafer submounted to the substrate. When the wafer was ground past the depth of the dicing and the grinding was complete you had chips mounted on a substrate. The wax did fill the dicing grooves and acted as a barrier once the grooves were reached from grinding. This reduced edge damage from grinding process. The thinnest I have been able to grind using this method is approx. 4 mils (101μm).

Problems

1. One problem with the dinger wax was chip movement. Reduced feed rates helped slightly.
2. The thicker stronger bond waxes had air pockets and were to viscous thus not allowing good squeeze out of adhesive.
3. The stronger bond adhesives tended to load the grinding wheel.
4. The stronger waxes are slightly harder to demount but not a roadblock.

Docket No. IRV1.PAU.30 **Patent Application**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :	Examiner: D. Graybill
Douglas M. Albert et al.	Group Art Unit: 3722
Serial No.: 09/190,378	
Filed: November 10, 1998	
For: METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine, California
	October 22, 2001

DECLARATION OF INVENTOR VOLKAN H. OZGUZ
SWEARING BEHIND REFERENCE
(37 CFR § 1.131)

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

I, Volkan H. Ozguz, hereby declare as follows:

1. I am an inventor in this application. I am making this declaration to establish facts showing that the invention claimed in this application was reduced to practice before February 7, 1996, which I am informed is the filing date of the application that issued to Alan J. Riding et al. as U.S. Patent No. 6,083,811 ('811 Patent). I will hereinafter refer to February 7, 1996 as the "Effective Date" of the '811 Patent.

2. I am employed by the assignee, Irvine Sensors Corporation ("ISC"). I work at ISC's Costa Mesa facility in the State of California. I have been employed continuously by ISC at all times relevant hereto

3. I have read Claims 1-32 that are pending in this application and have a technical understanding of how such claims apply to the disclosure of this application.

4. As a co-inventor, I actively collaborated with Mr. Albert in the development of the claimed invention and am personally familiar with the development of the invention claimed in our patent application. I have reviewed the fully-executed DECLARATION OF DOUGLAS M. ALBERT SWEARING BEHIND REFERENCE, including Exhibits "A" and "B" attached thereto. I hereby adopt and incorporate by reference the content of paragraphs 4 to 6 of Mr. Albert's declaration and the attached Exhibits "A" and B", as if such descriptions were fully set forth herein and such exhibits were attached hereto.

5. This declaration factually establishes that the claimed invention was reduced to practice in the United States prior to the Effective Date of the '811 Patent.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

10/19/2001.
Date

Volkan H. Ozguz

Atty. Dkt. No.: IRV1.PAU.30 **PATENT APPLICATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Douglas M. Albert et al.	Examiner:	D. Graybill
Serial No.:	09/190,378	Art Unit:	2814
Filed:	November 10, 1998		
Title:	METHOD FOR THINNING SEMICONDUCTOR WAFERS WITH CIRCUITS AND WAFERS MADE BY THE SAME	Irvine California	
		October 22, 2001	

REQUEST FOR THREE-MONTH EXTENSION OF TIME

Assistant Commissioner for Patents
Washington, DC 20231

Dear Sir:

Applicants request a three-month extension of time from July 20, 2001 to October 22, 2001 to respond to the Office Action of April 20, 2001.

Our check in the amount of $460.00 to cover the fee for such an extension of time is enclosed.

Please charge any additional fees to our Deposit Account No. 01-1960. One copy of this letter is enclosed for such purpose.

Certificate of Mailing
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231 on October 22, 2001

By Angela Williams

A. Williams
Signature
October 22, 2001

Respectfully submitted,

Joseph C. Andras
Registration No. 33,469
Myers, Dawes & Andras
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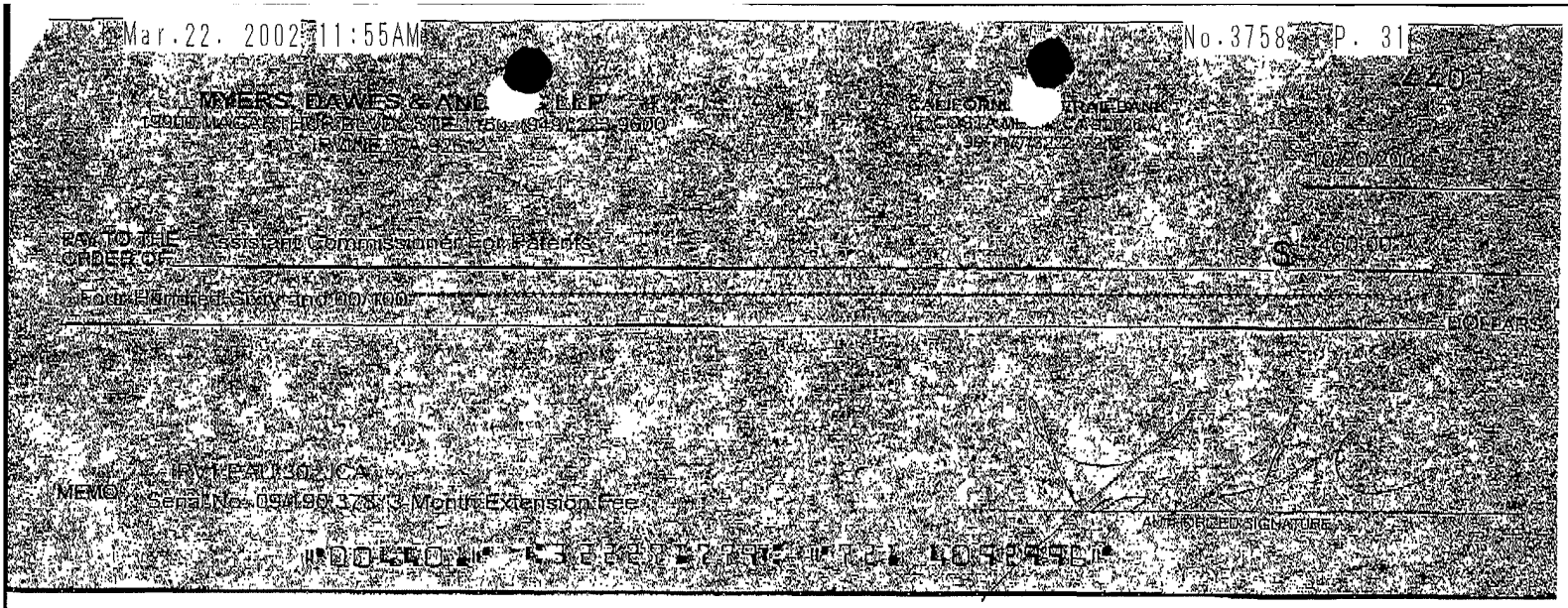
(949) 223-9600



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